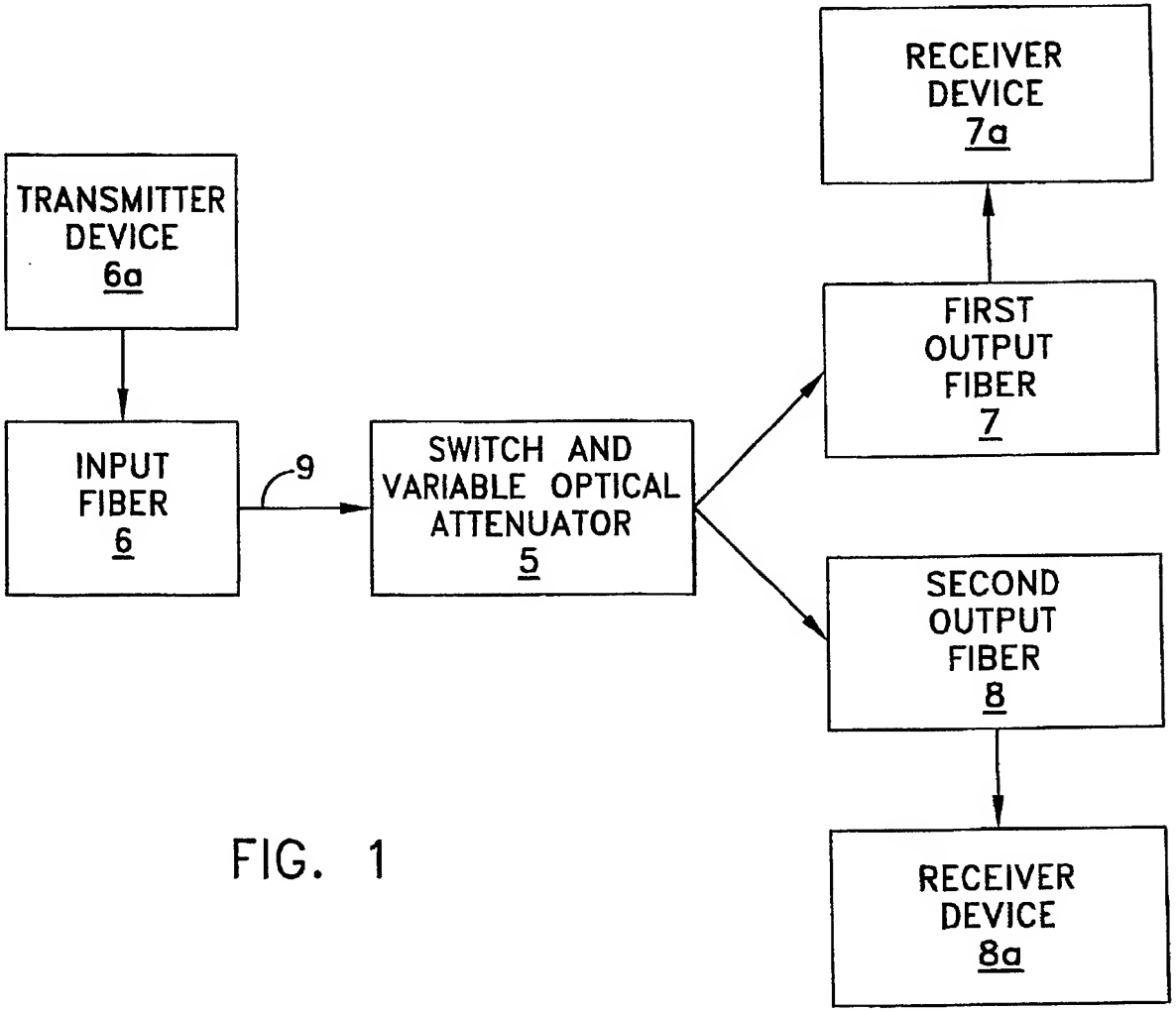

FIG. 1

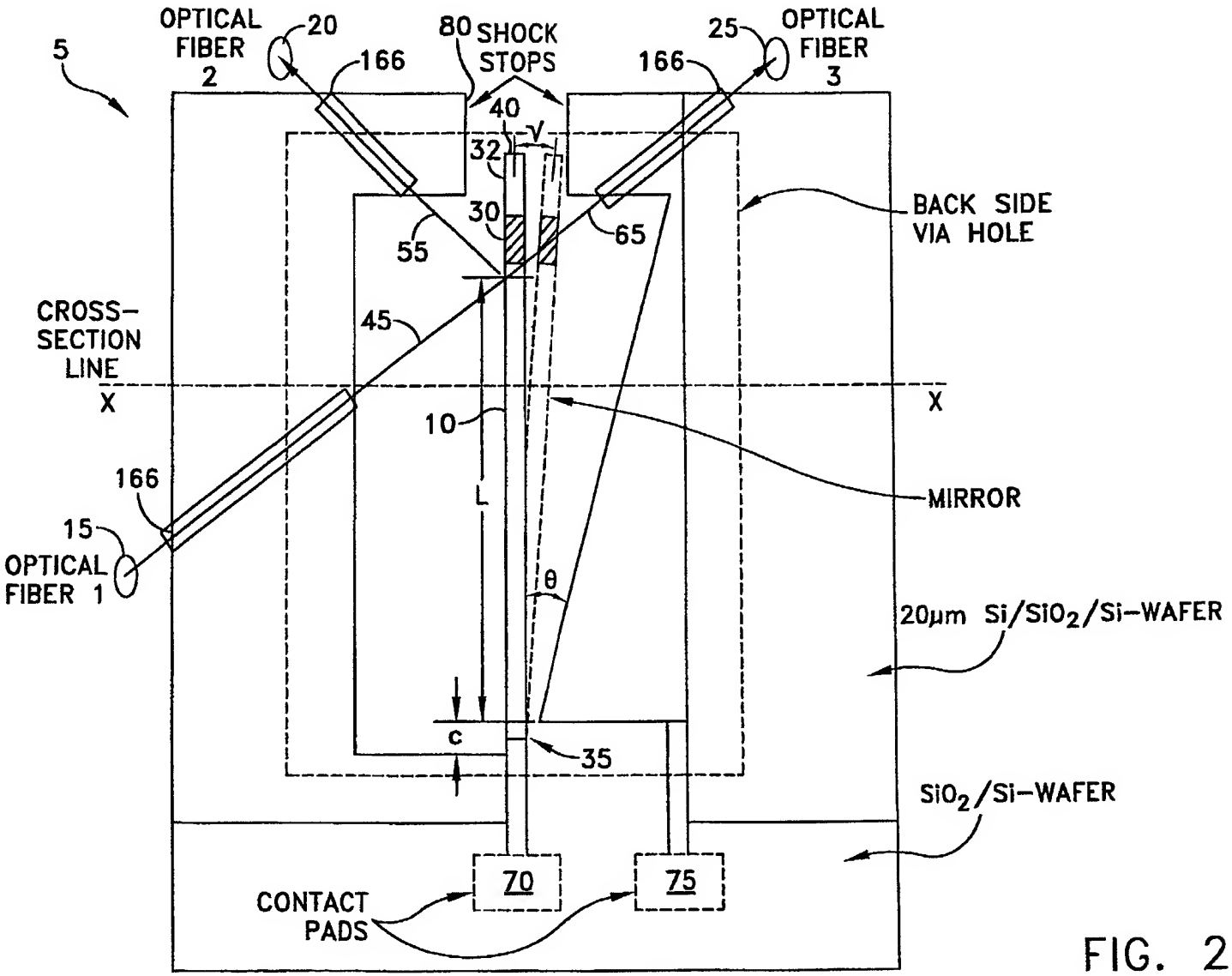

FIG. 2

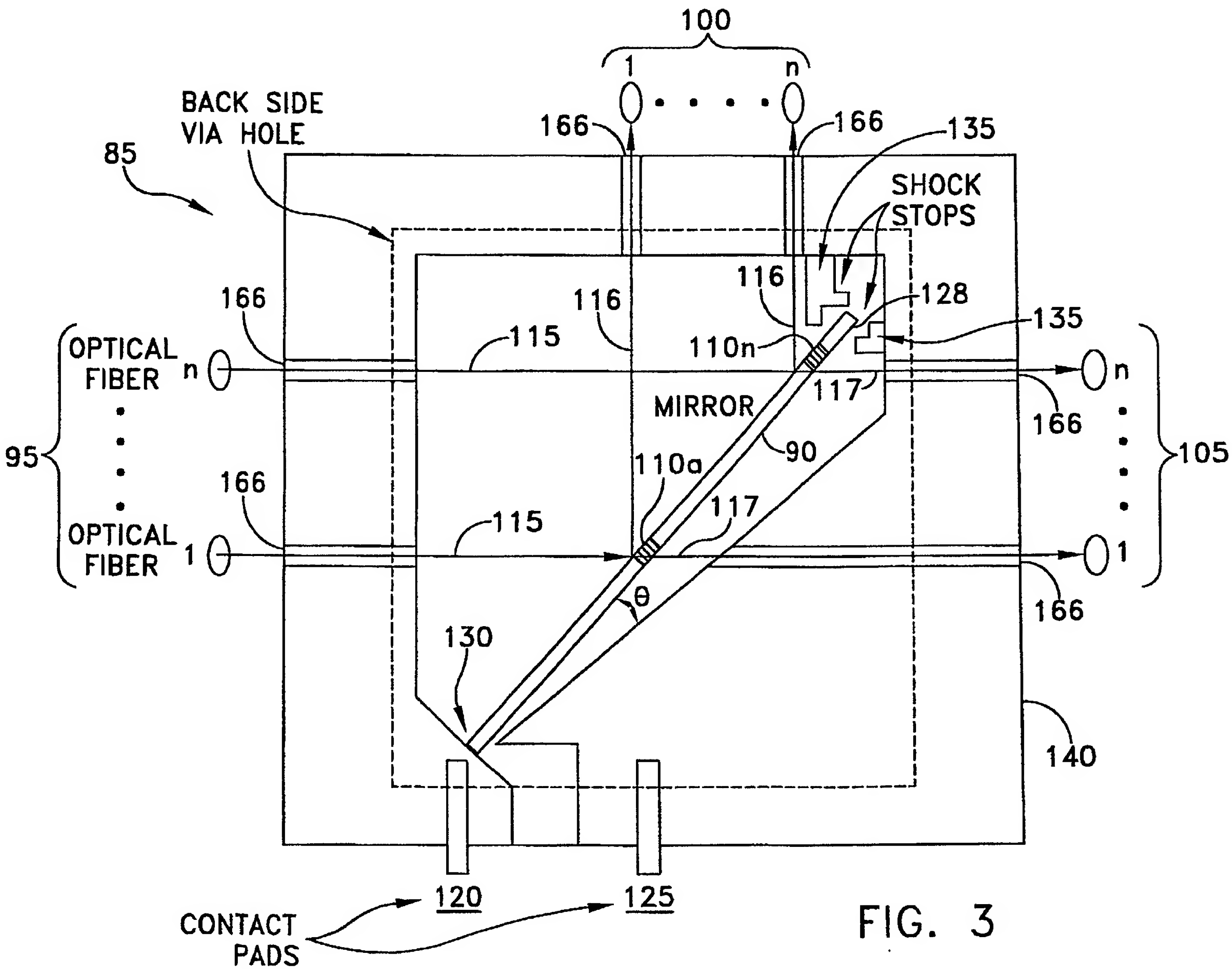
100
1
n
166
166
135
BACK SIDE
VIA HOLE
85
SHOCK
STOPS
116
128
166
116
135
115
OPTICAL
FIBER
n
110n
n
117
MIRROR
166
95
90
105
110a
166
117
115
OPTICAL
FIBER
1
1
θ
166
130
140
120
125
CONTACT
PADS

FIG. 3

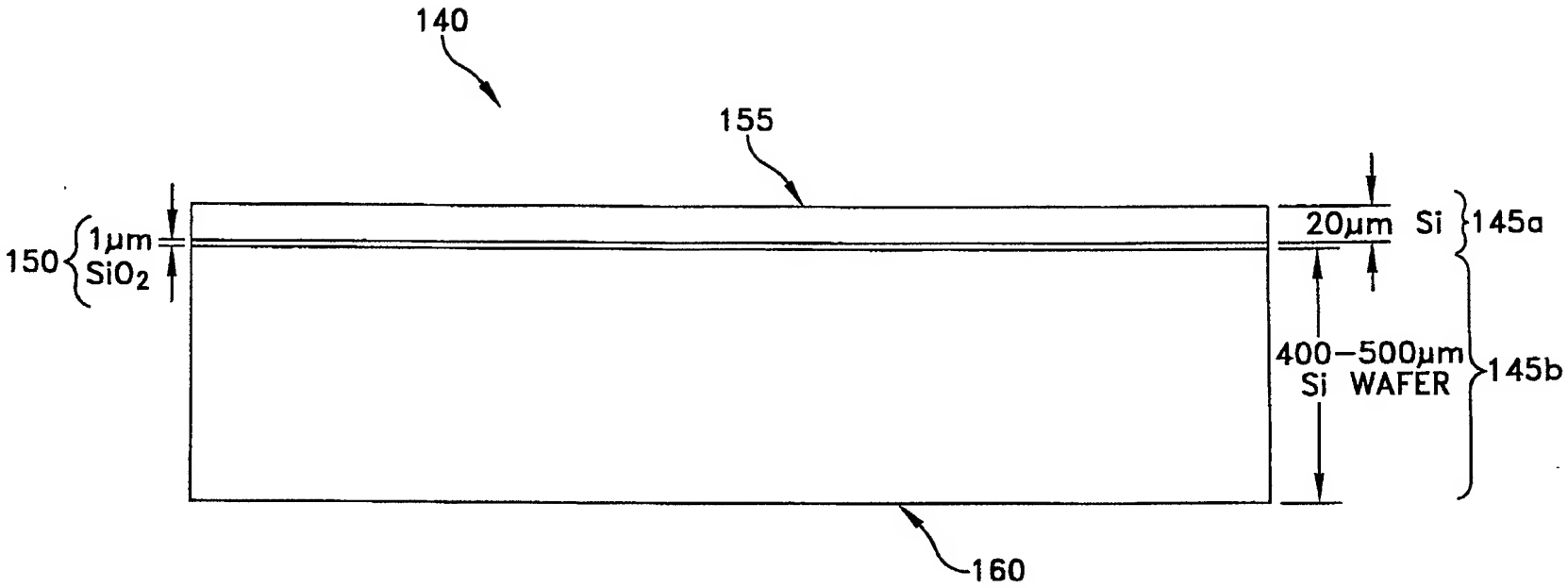

FIG. 4a

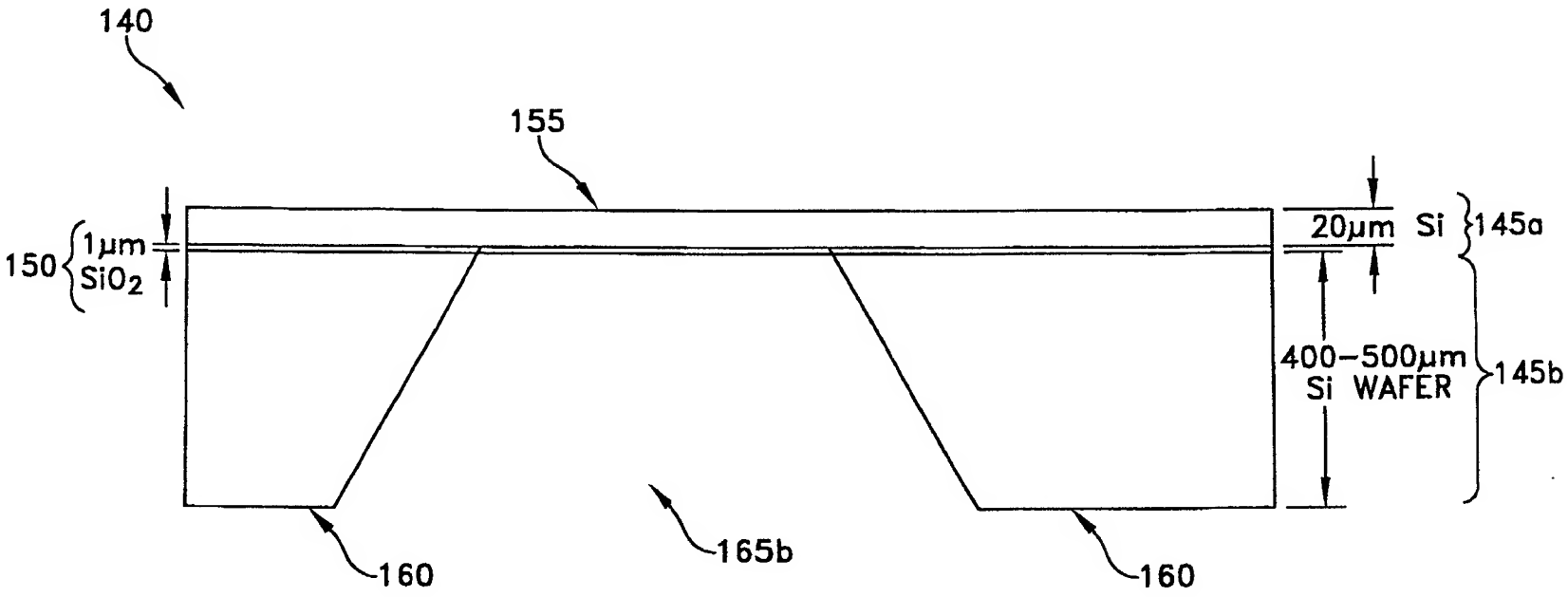

FIG. 4b

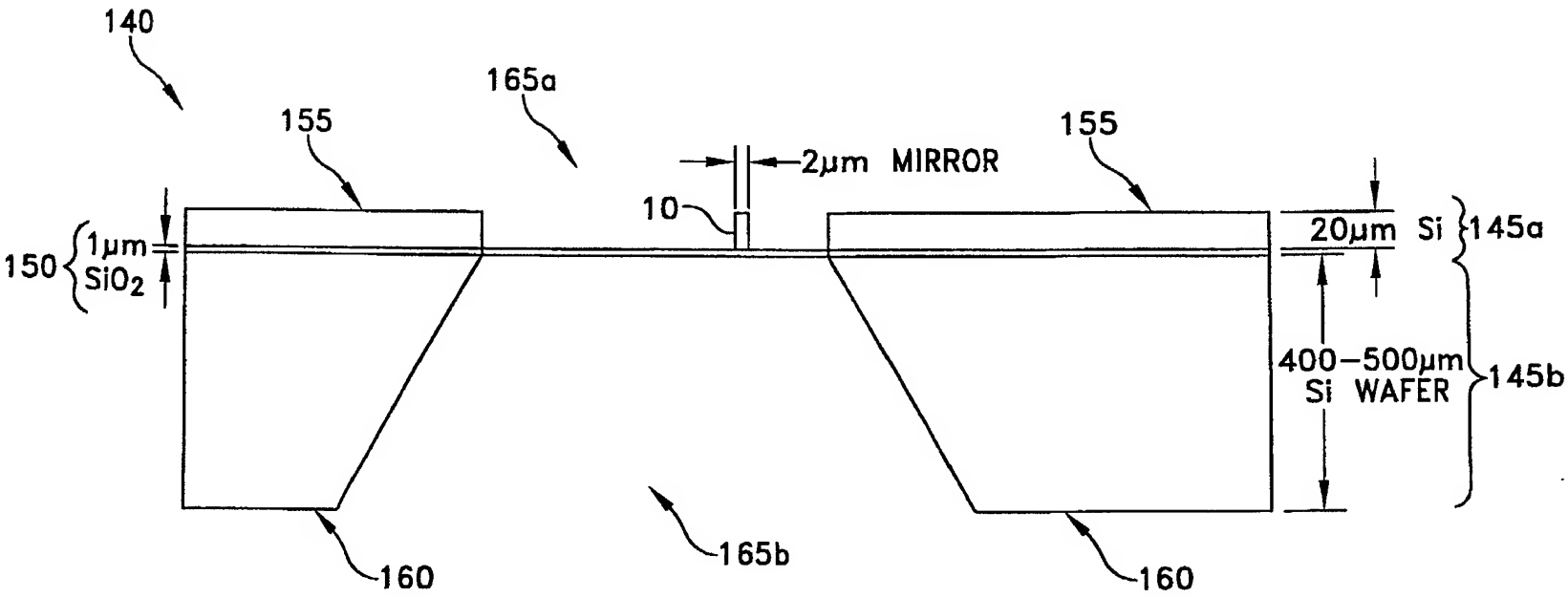

FIG. 4c

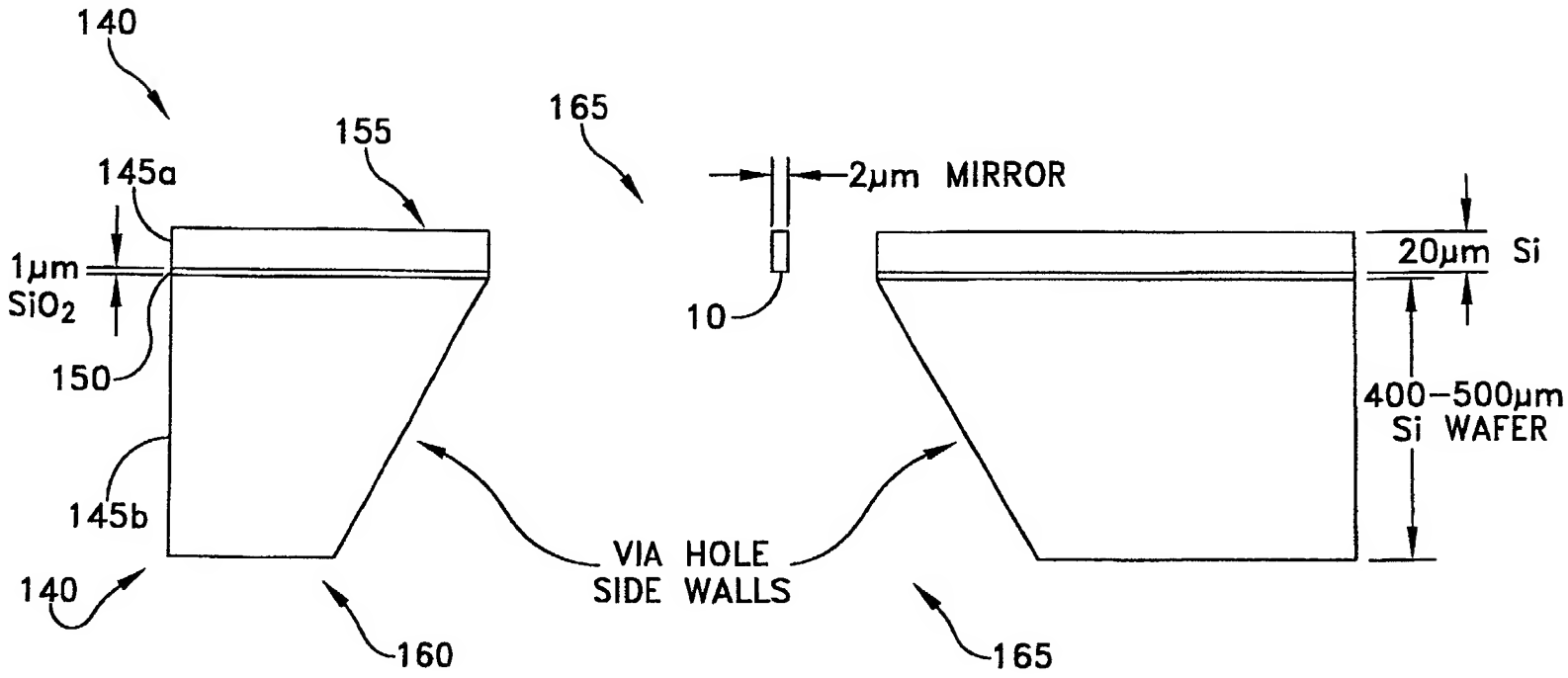

FIG. 4d

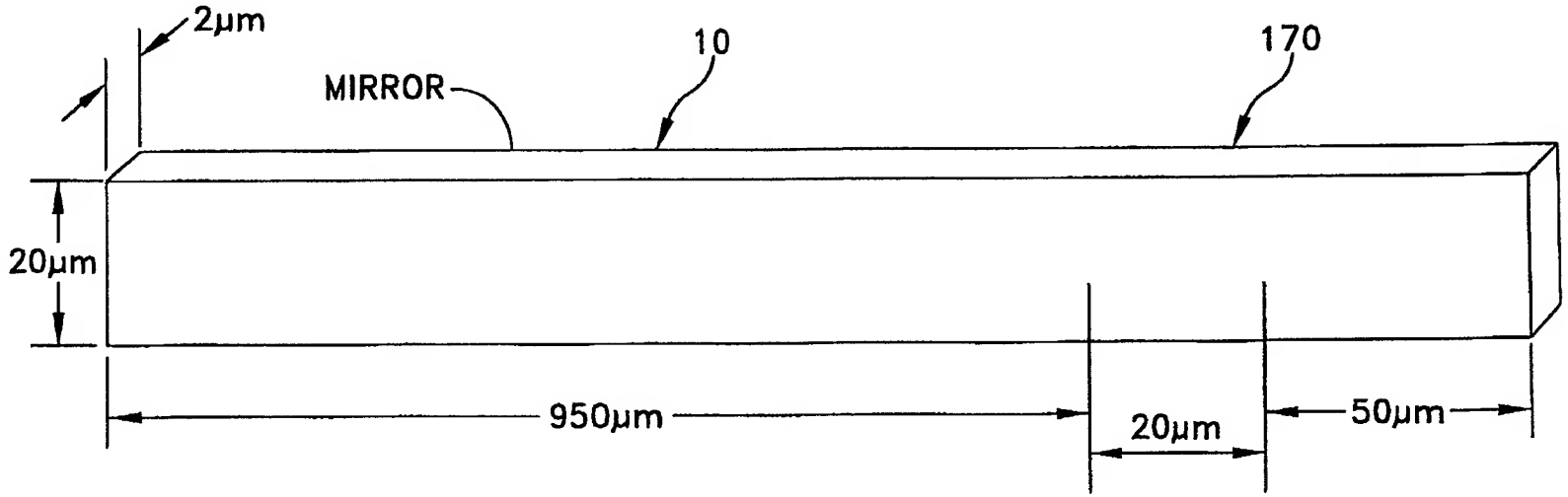

FIG. 5a

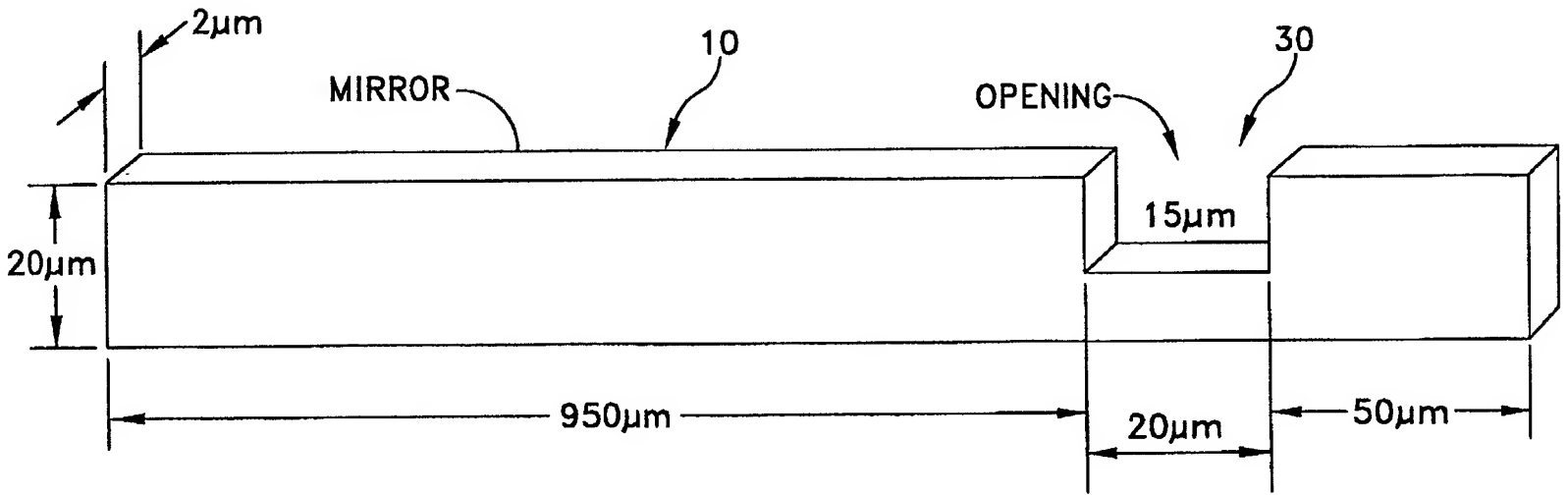

FIG. 5b

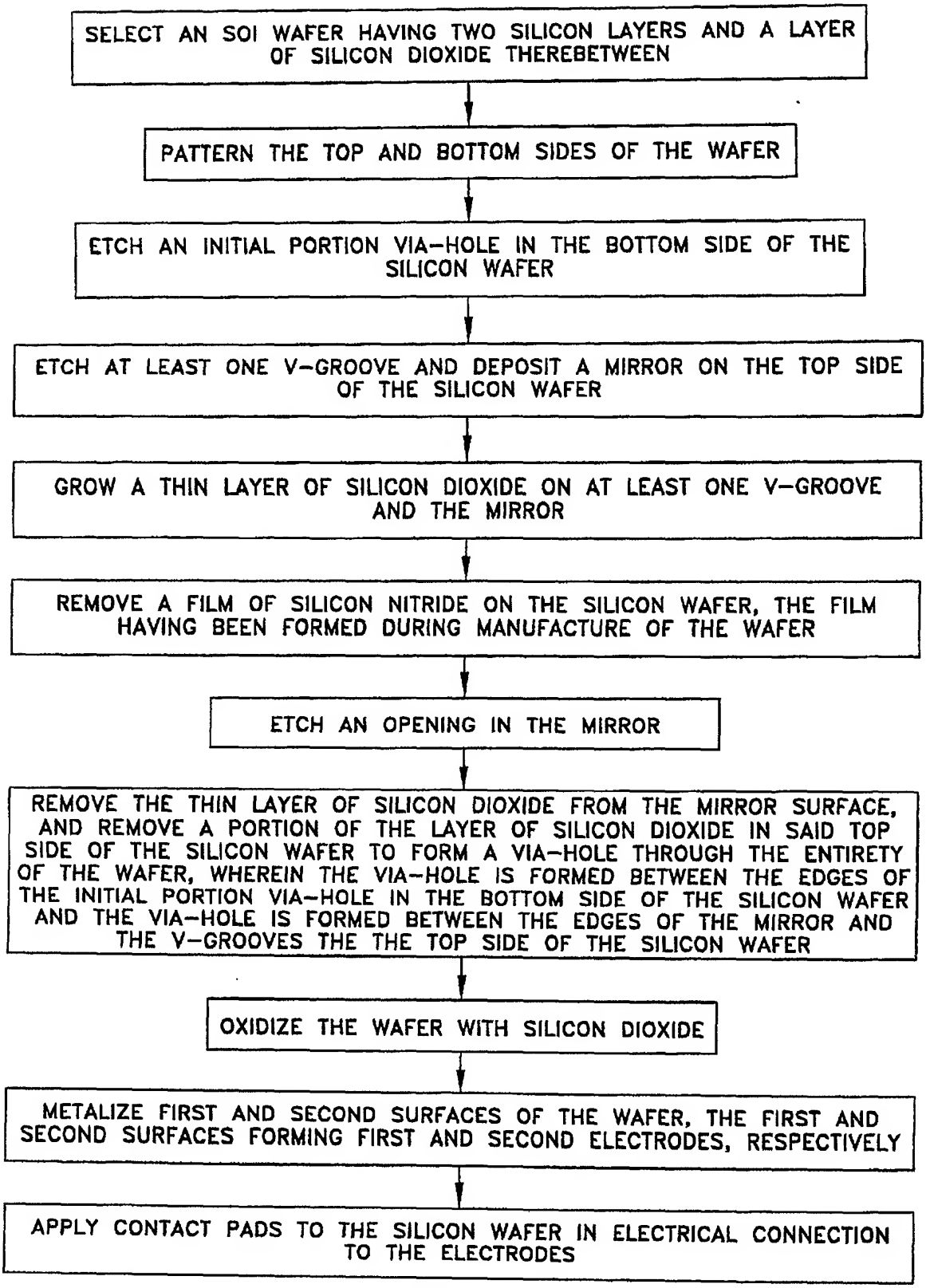
SELECT AN SOI WAFER HAVING TWO SILICON LAYERS AND A LAYER OF SILICON DIOXIDE THEREBETWEEN
PATTERN THE TOP AND BOTTOM SIDES OF THE WAFER
ETCH AN INITIAL PORTION VIA-HOLE IN THE BOTTOM SIDE OF THE SILICON WAFER
ETCH AT LEAST ONE V-GROOVE AND DEPOSIT A MIRROR ON THE TOP SIDE OF THE SILICON WAFER
GROW A THIN LAYER OF SILICON DIOXIDE ON AT LEAST ONE V-GROOVE AND THE MIRROR
REMOVE A FILM OF SILICON NITRIDE ON THE SILICON WAFER, THE FILM HAVING BEEN FORMED DURING MANUFACTURE OF THE WAFER
ETCH AN OPENING IN THE MIRROR
REMOVE THE THIN LAYER OF SILICON DIOXIDE FROM THE MIRROR SURFACE, AND REMOVE A PORTION OF THE LAYER OF SILICON DIOXIDE IN SAID TOP SIDE OF THE SILICON WAFER TO FORM A VIA-HOLE THROUGH THE ENTIRETY OF THE WAFER, WHEREIN THE VIA-HOLE IS FORMED BETWEEN THE EDGES OF THE INITIAL PORTION VIA-HOLE IN THE BOTTOM SIDE OF THE SILICON WAFER AND THE VIA-HOLE IS FORMED BETWEEN THE EDGES OF THE MIRROR AND THE V-GROOVES THE THE TOP SIDE OF THE SILICON WAFER
OXIDIZE THE WAFER WITH SILICON DIOXIDE
METALIZE FIRST AND SECOND SURFACES OF THE WAFER, THE FIRST AND SECOND SURFACES FORMING FIRST AND SECOND ELECTRODES, RESPECTIVELY
APPLY CONTACT PADS TO THE SILICON WAFER IN ELECTRICAL CONNECTION TO THE ELECTRODES

FIG. 6